BCT642A
2:1 MIPI D-PHY,C-PHY(2.5Gbps) 2-Data Lane Switch

GENERAL DESCRIPTION

The BCT642A is a two-data-lane, MIPI, D-PHY, C-PHY switch. This single-pole, double-throw (SPDT) switch is optimized for switching between two high-speed or low-power MIPI sources. The BCT642A is designed for the MIPI specification and allows connection to a CSI or DSI module.

APPLICATIONS

Cellular Phones, Smart Phones
Displays

FEATURES

- Switch Type: SPDT(6x)
- Signal Types: MIPI, D-PHY,C-PHY
- V_{CC}:1.65 to 4.5V
- R_{ON}: 6.0Ω Typical HS MIPI
  7.0Ω Typical LP MIPI
- ΔR_{ON}: 0.6Ω Typical
- R_{ON_FLAT}: 0.3Ω Typical
- I_{CC}: 26uA Typical
- Differential Bandwidth:2.5GHz Typical
- C_{ON}:5.0pF
- QFN3.4x2.5-24L Package

ORDERING INFORMATION

Order Number	Package Type	Temperature Range	Marking	QTY/Reel
BCT642AEGG-TR	QFN3.4x2.5-24L	-40°C to +85°C	642A XXXXX	3000

Mark Note:
1. "642A" in Marking is Product code
2. "XXXXX" in Marking will be appeared as the batch code.

PIN CONFIGURATION

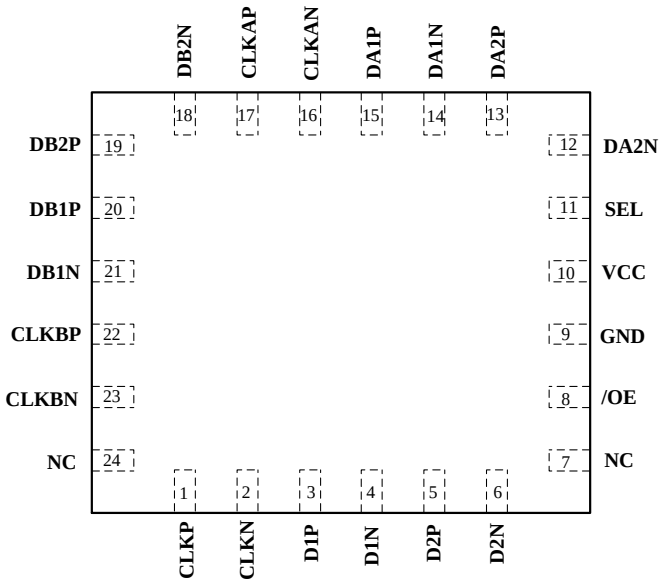


Figure1. Pin Configuration(Top Through View)

PIN DESCRIPTION

PIN	NAME	FUNCTION
1, 2	CLKP, CLKN	Clock Path (Common)
3, 4	D1P, D1N	Data Path 1 (Common)
5, 6	D2P, D2N	Data Path2 (Common)
7, 24	NC	No Connect (Float)
8	/OE	Output Enable (Active Low)
9	GND	Ground
10	VCC	Power
11	SEL	Select (0=A,1=B)
12, 13	DA2N, DA2P	Data Path (A2)
14, 15	DA1N, DA1P	Data Path (A1)
16, 17	CLKAN, CLKAP	Clock Path (A)
18, 19	DB2N, DB2P	Data Path (2B)
20, 21	DB1P, DB1N	Data Path (1B)
22, 23	CLKBP, CLKBN	Clock Path (B)

FUNCTIONAL DIAGRAM

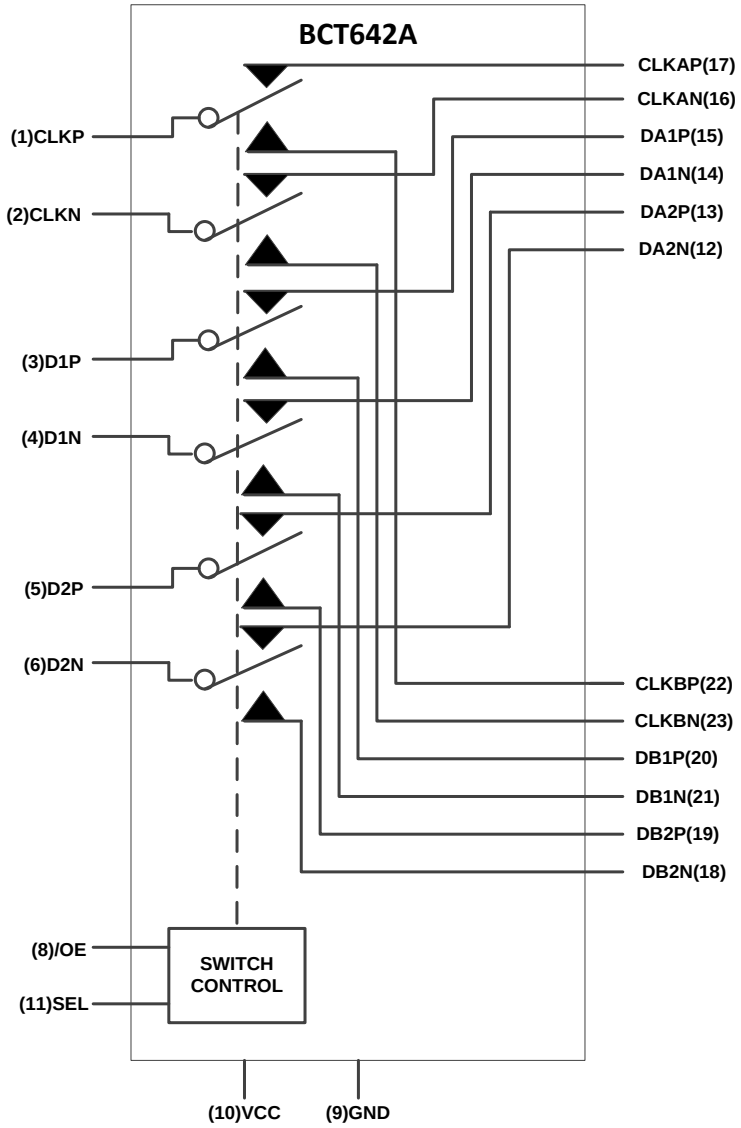


Figure2. Functional Diagram

TRUTH TABLE

SEL	/OE	Function
Don't care	HIGH	Disconnect
LOW	LOW	D1, D2, CLK=DA1, DA2, CLKA
HIGH	LOW	D1, D2, CLK=DB1, DB2, CLKB

TYPICAL OPERATING CIRCUIT

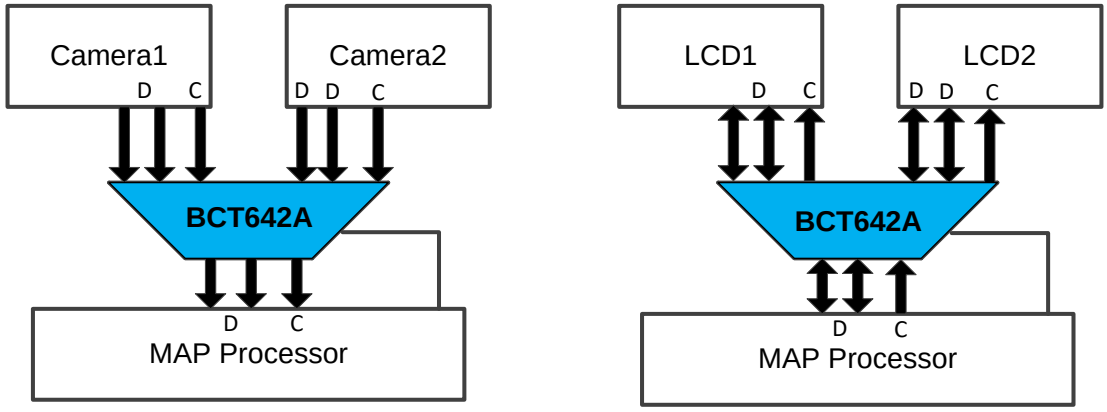


Figure 3. Application Block Diagram

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC})….....-0.5V to +5.25V
DC Input Voltage (SEL, /OE)[1].....-0.5V to +5.25V
DC Switch I/O Voltage.....-0.5V to 5.25V
DC Input Diode Current.....-50mA
DC Output Current …….....50mA
Storage Temperature Range.....-65℃ to +150℃
Junction Temperature.....150℃
Operating Temperature Range.....-40℃ to +85℃
Lead Temperature (Soldering, 10 sec).....260℃
ESD Susceptibility
All Pins.....2KV

CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. Broadchip recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Broadchip reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact Broadchip sales office to get the latest datasheet.

RECOMMENDED OPERATING CONDTIONS

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		1.65	4.5	V
V_{CTRL}	Control Input Voltage(SEL, /OE)[2]		0	V_{CC}	V
V_{SW}	Switch I/O Voltage (CLKn, CLKAn, CLKBn, Dn, DAn, DBn)	HS Mode	0.1	0.3	V
		LP Mode	0	1.2	
T_A	Operating Temperature		-40	+85	℃

Notes：

1. The input and output negative ratings maybe exceed if the input and output diode current ratings are observed.
2. The control input must be held HIGH or LOW; it must not float.

DC ELECTRICAL CHARACTERISTICS

(All typical values are T_A = 25℃, unless otherwise specified.)

PARAMETER	SYM	CONDITIONS	V_{CC} (V)	MIN	TYP	MAX	UNITS
Control Input Leakage(SEL, /OE)	I_{IN}	V_{SW}=0 to 1.3V	1.65 to 4.5	-1		1	uA
Input Voltage High	V_{IH}	V_{IN}=0 to V_{CC}	1.65 to 4.5	1.0			V
Input Voltage Low	V_{IL}	V_{IN}=0 to V_{CC}	1.65 to 4.5			0.4	V
Off leakage Current of Port CLKAn, DAn, CLKBn, DBn	$I_{NO(OFF)}$ $I_{NC(OFF)}$	CLKn, Dn=0.3V; V_{CC}-0.3V; CLKAn, DAn, or CLKBn; DBn=V_{CC}-0.3V, 0.3V, or Floating; /OE=0V	1.65 to 4.5	-1		1	uA
On leakage Current of Common Ports(CLKAn, Dn)	$I_{A(ON)}$	CLKn, Dn=0.3V; Vcc-0.3V; CLKAn, DAn, or CLKBn; DBn=V_{CC}-0.3V, 0.3V, or Floating; /OE=0V	1.65 to 4.5	-1		1	uA
Power-Off Leakage Current	I_{OFF}	CLKn, Dn or CLKAn, DAn, or CLKBn; DBn; V_{IN}=0V to 4.5V; V_{CC}=0V	0	-1		1	uA
Off-State Leakage	I_{OZ}	0≤CLKn, Dn, CLKAn, DAn, CLKBn, DBn≤ 3.6V; /OE=High	4.5	-1		1	uA
Switch On Resistance for HS MIPI Applications(3)	$R_{ON\_MIPI\_HS}$	I_{ON}=-10mA, /OE=0V, SEL=V_{CC} or 0V, $CLK_{A, B}$, DBn or DAn=0.1, 0.2, 0.3	1.8--4.5		6.0		Ω
Switch On Resistance for LP MIPI Applications(3)	$R_{ON\_MIPI\_LP}$	I_{ON}=-10mA, /OE=0V, SEL=V_{CC} or 0V, $CLK_{A, B}$, DBn or DAn=0, 0.6, 1.2V	1.8-4.5		7.0		Ω
On Resistance Matching Between HS MIPI Channels(4)	$\Delta R_{ON\_MIPI\_HS}$	I_{ON}=-10mA, /OE=0V, SEL=V_{CC} or 0V, $CLK_{A, B}$, DBn or DAn=0.1, 0.2, 0.3	1.8-4.5		0.6		Ω

DC ELECTRICAL CHARACTERISTICS

(All typical values are T_A = 25℃, unless otherwise specified.)

PARAMETER	SYM	CONDITIONS	V_{CC} (V)	MIN	TYP	MAX	UNITS
On Resistance Matching Between LP MIPI Channels(4)	$\Delta R_{ON\_MIPI\_LP}$	I_{ON}=-10mA, /OE=0V, SEL=V_{CC} or 0V, $CLK_{A, B}$, DBn or DAn=0.0, 0.6, 1.2V	1.8-4.5		0.6		Ω
On Resistance Flatness for HS MIPI Signals(4)	$R_{ON\_FLAT\_MIPI\_HS}$	I_{ON}=-10mA, /OE=0V, SEL=V_{CC} or 0V, $CLK_{A, B}$, DBn or DAn=0.1, 0.2, 0.3	1.8-4.5		0.3		Ω
On Resistance Flatness for LP MIPI Signals(4)	$R_{ON\_FLAT\_MIPI\_LP}$	I_{ON}=-10mA, /OE=0V, SEL=V_{CC} or 0V, $CLK_{A, B}$, DBn or DAn=0.0, 0.6, 1.2V	1.8-4.5		1.5		Ω
Quiescent Hi-Z Supply Current	I_{CCZ}	$V_{/OE}$= V_{CC} ,V_{IN}=0 or V_{CC}, I_{OUT}=0	4.5			0.5	uA
Quiescent Supply Current	I_{CC}	$V_{/OE}$= 0 ,V_{IN}=0 or V_{CC}, I_{OUT}=0	2.8		26		uA
Increase in I_{CC} Current Per Control Voltage and V_{CC}	I_{CCT}	$V_{SEL, /OE}$=1.65V	4.5		4.0		uA
			2.5		0.1		

Notes:

3. Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the two (A or B ports).
4. Guaranteed by characterization

AC ELECTRICAL CHARACTERISTICS

(All values are for V_{CC}=3.3V at T_A=25℃ unless otherwise specified.)

PARAMETER	SYM	CONDITIONS	V_{CC} (V)	MIN	TYP	MAX	UNITS
Initalization Time VCC to Output(5)	t_{INIT}	R_L=50Ω, C_L=5pF, V_{SW}=1.2V	2.5 to 4.5			100	us
			1.8			150	
Enable Turn-On Time, /OE to Output	t_{EN}	R_L=50Ω, C_L=5pF, V_{SW}=1.2V	2.5 to 4.5		120	200	ns
			1.8		250	500	
Disable Turn-off Time, /OE to Output	t_{DIS}	R_L=50Ω, C_L=5pF, V_{SW}=1.2V	2.5 to 4.5		25	50	ns
			1.8		50	90	
Turn-On Time SEL to Output	t_{ON}	R_L=50Ω, C_L=5pF, V_{SW}=1.2V	2.5 to 4.5		50	100	ns
			1.8		75	125	

AC ELECTRICAL CHARACTERISTICS

(All values are for V_{CC}=3.3V at T_A=25℃ unless otherwise specified.)

PARAMETER	SYM	CONDITIONS	V_{CC} (V)	MIN	TYP	MAX	UNITS
Turn-Off Time SEL to Output	t_{OFF}	R_L=50Ω, C_L=5pF, V_{SW}=1.2V	2.5 to 4.5		50	200	ns
			1.8		200	325	
Break-Before-Make Time	t_{BBM}	C_L=5pF, R_L=50Ω, V_{SW}=1.2V		10	50		ns
Off Isolation for MIPI(5)	O_{IRR}	f=750MHz, R_L=50Ω, /OE=V_{CC} ,V_{SW}=-1dBm (200mV_{PP})	1.65 to 4.5		-32		dB
Crosstalk for MIPI(5)	Xtalk	f=750MHz, R_L=50Ω, /OE=V_{CC} ,V_{SW}=-1dBm (200mV_{PP})	1.65 to 4.5		-35		dB
Differential -3db Bandwidth(5)	BW	C_L=0pF, R_L=50Ω	3.0	2.0	2.5		GHz

Note:
5. Guaranteed by characterization.

HIGH-SPEED-RELATED AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYM	CONDITIONS	V_{CC} (V)	MIN	TYP	MAX	UNITS
Channel-to-Channel Single-Ended Skew(6)	$t_{SK(O)}$	TDR-Based Method (V_{SW}=0.2V_{PP}, C_L=C_{ON})	3.3		6	20	ps
Skew of Opposite Transitions of the Same Output(6)	$t_{SK(P)}$	TDR-Based Method (V_{SW}=0.2V_{PP}, C_L=C_{ON})	3.3		6	20	ps

Notes:
6. Guaranteed by characterization.

CAPACITANCE

PARAMETER	SYM	CONDITIONS	V_{CC} (V)	MIN	TYP	MAX	UNITS
Control Pin Input Capacitance(7)	C_{IN}	V_{CC}=0V, f=1MHz	0		2.1		pF
Output On Capacitance(7)	C_{ON}	V_{CC}=3.3V, /OE=0V, f=1MHz	3.3		5.0		
Output Off Capacitance(7)	C_{OFF}	V_{CC} and /OE=3.3V, f=1MHz	3.3		2.0		

Note:
7. Guaranteed by characterization.

TEST DIAGRAMS

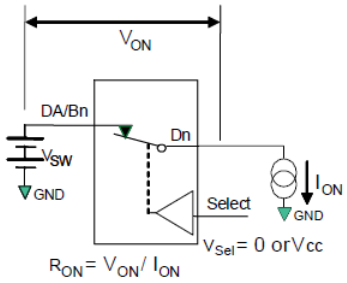


Figure 4. On Resistance

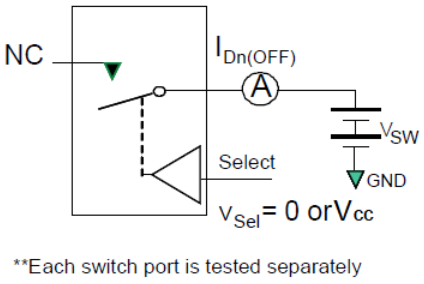


Figure 5. Off Leakage

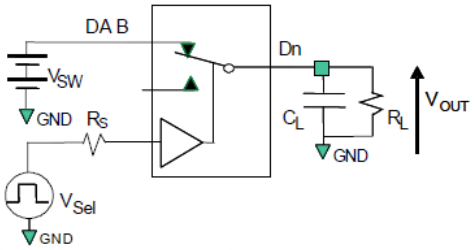


Figure 6. AC Test Circuit Board

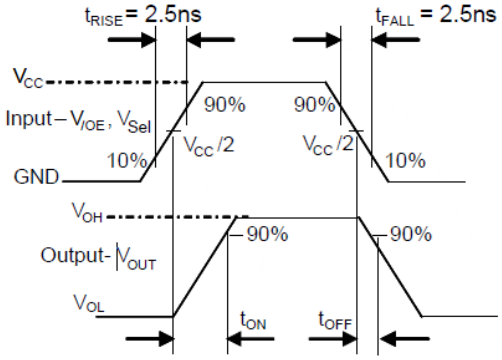


Figure 7. Turn-On/Turn-Off waveform

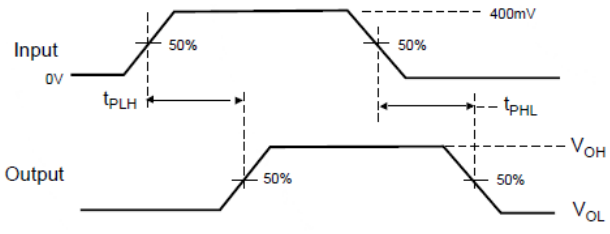


Figure 8. Propagation Delay($t_R$$t_F$-500ps)

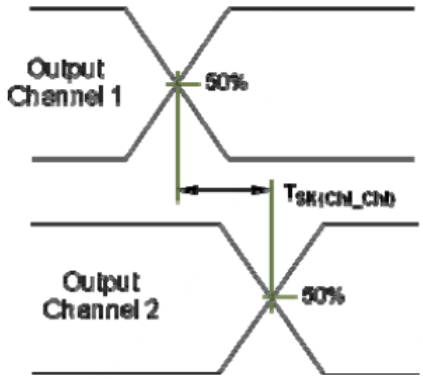


Figure 9. Channel to Channel Skew

TEST DIAGRAMS (CONTINUED)

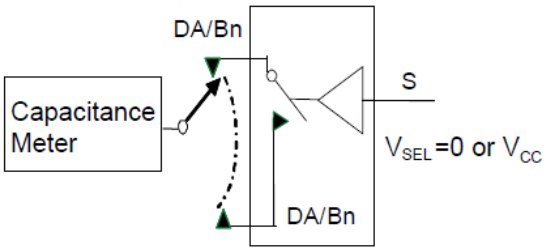


Figure 10. Channel Off Capacitance

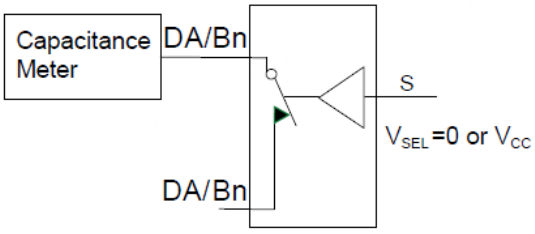


Figure 11. Channel On Capacitance

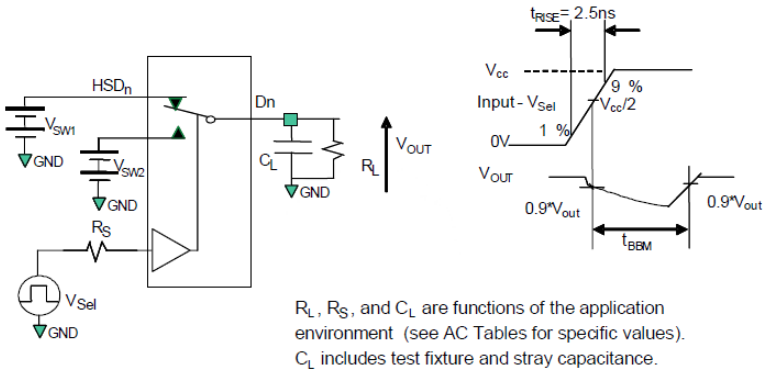
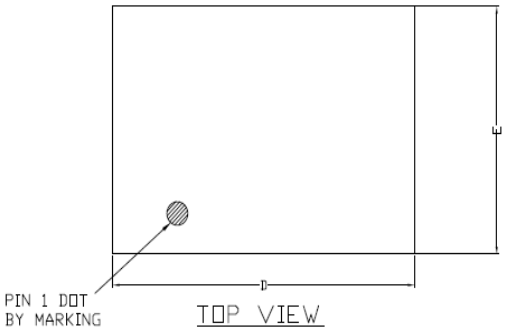


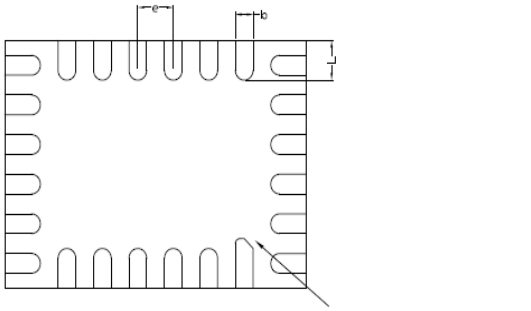
Figure 12. Break-Before-Make Interval Timing

PACKAGE OUTLINE DIMENSIONS

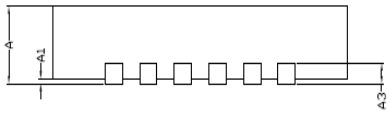
QFN3.4x2.5-24L



TOP VIEW



BOTTOM VIEW



SIDE VIEW

COMMON DIMENSIONS(MM)			
PKG.	W\VERY VERY THIN		
REF.	MIN.	NOM.	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3		0.2 REF.	
D	3.35	3.40	3.45
E	2.45	2.50	2.55
b	0.15	0.20	0.25
L	0.30	0.40	0.50
e	0.40 BSC		

RECOMMEDNED PCB LAYOUT PATTERN (UNIT:mm)