

# BCT4567

## Low-Power, Dual SIM Card Analog Switch

### GENERAL DESCRIPTION

The BCT4567 is a QPDT switch with one common control inputs targeted at dual SIM card multiplexing. It is optimized for switching the WLAN-SIM data and control signals and dedicates one channel as a supply-source switch.

The switches are fully bi-directional, allowing both multiplexing and de-multiplexing operation. Break-before-make operation is guaranteed.

The device operates from a +1.65V to +5.0V supply and over the extended -40°C to +85°C temperature range. It is offered in 16-pin 3mm x 3mm TQFN package or 16-pin 1.8mm x 2.6mm UTQFN package.

### APPLICATIONS

Dual SIM Card Switch  
Cell Phones  
Pad  
Digital Cameras  
PDAs  
Notebook

### FEATURES

- Low 0.5Ω Ron @VCC=2.7V
- 0.06Ω On-Resistance Flatness
- Excellent 0.05Ω On-Resistance Matching
- Wide VCC Operating Range: 1.65 V to 5.0V
- Rail-to-Rail Signal Switching Range
- Fast Switching Speed: 20nsTYP at 3.3V
- High Off Isolation: -66dB
- Crosstalk Rejection: -86dB
- -3dB bandwidth: 100MHz
- Space-Saving, TQFN 3x3-16L or QFN2.6x1.8-16L Package

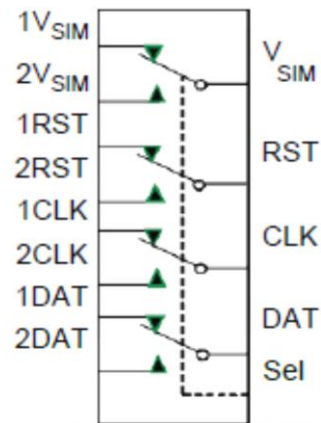



Figure 1. Analog Symbol

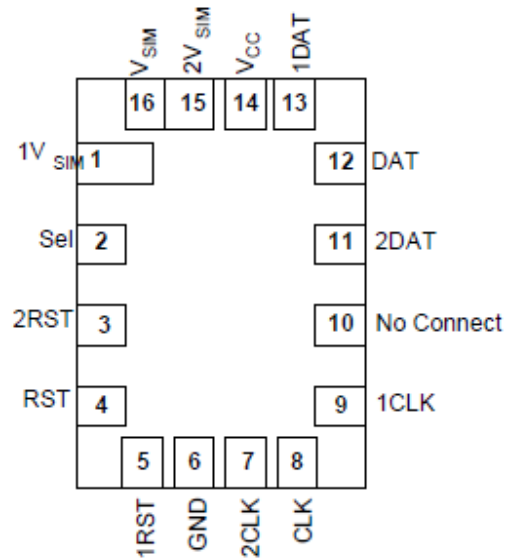
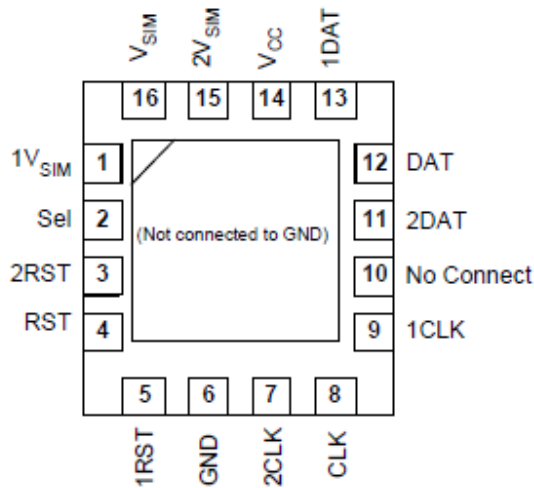
### ORDERING INFORMATION

Ordering Code	Package Description	Temp Range	Top Marking	QTY/Reel
BCT4567EGE-TR	TQFN3x3-16L	-40°C to +85°C	 XXXXX 4567	3000
BCT4567EFE-TR	QFN2.6x1.8-16L	-40°C to +85°C	XXXX 4567	3000

Mark Note:

1. "4567" in Marking is product short code for BCT4567.
2. "XXXXX" in Marking will be appeared as the batch code.

### Pin Configurations



### Pin Description

Pin	Name	Function
1	1VSIM	SIM supply output 1
2	SEL	Select input
3	2RST	RST Normally Open Terminal
4	RST	RST Common Terminal
5	1RST	RST Normally Closed Terminal
6	GND	Ground
7	2CLK	CLK Normally Open Terminal
8	CLK	CLK Common Terminal
9	1CLK	CLK Normally Closed Terminal
10	NC	Not Connect
11	2DAT	DAT Normally Open Terminal
12	DAT	DAT Common Terminal
13	1DAT	DAT Normally Closed Terminal
14	VCC	Power Supply
15	2VSIM	SIM supply output 2
16	VSIM	SIM supply input

### Truth Table

SEL	SWITCH STATE
0	1DAT = DAT, 1RST = RST, 1CLK = CLK, 1V <sub>SIM</sub> = V <sub>SIM</sub>
1	2DAT = DAT, 2RST = RST, 2CLK = CLK, 2V <sub>SIM</sub> = V <sub>SIM</sub>

### Absolute Maximum Ratings

VCC, SEL to GND.....	-0.3V to +6.0V
All Other Pins to GND.....	-0.3V to (VCC + 0.3V)
Continuous Current .....	±400mA
Peak Current (pulsed at 1ms, 10% duty cycle) .....	±500mA
Continuous Power Dissipation (TA = +70°C) ( 15.6mW/°C above +70°C) .....	1.25W
Operating Temperature Range .....	-40°C to +85°C
Storage Temperature Range.....	-65°C to +150°C
Junction Temperature.....	+150°C
Lead Temperature (soldering, 10s).....	+260°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### Electrical Characteristics

(unless otherwise noted. Typical values are at VCC = 3.3V, TA = +25°C. (Note 2))

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>POWER SUPPLY</b>						
Supply Voltage Range	VCC		1.65		5.0	V
Supply Current	ICC	V <sub>CNTRL</sub> = 0 or V <sub>CC</sub> , I <sub>OUT</sub> = 0			1.0	µA
<b>ANALOG SWITCH</b>						
Analog Signal Range	V <sub>SW</sub>	Switch I/O Voltage	0		VCC	V
On-Resistance	RON	I <sub>ON</sub> = -100 mA Figure 9	VCC = 1.8V V <sub>SW</sub> = 0, 1.8 V	0.8		Ω
			VCC = 2.7V V <sub>SW</sub> = 0, 2.3 V	0.5		
On-Resistance Match	ΔRON	I <sub>ON</sub> = -100 mA Figure 9	VCC = 1.8V V <sub>SW</sub> = 0, 1.8 V	0.1		Ω
			VCC = 2.7V V <sub>SW</sub> = 0, 2.3 V	0.05		
On-Resistance Flatness	RFLAT	I <sub>ON</sub> = -100 mA Figure 9	VCC = 1.8V V <sub>SW</sub> = 0, 1.8 V	0.12		Ω
			VCC = 2.7V V <sub>SW</sub> = 0, 2.3 V	0.06		
Off-Leakage Current	I <sub>OFF</sub>	VCC = 4.3V, nRST, nDAT, nCLK, nVSIM = 0.3 V or 3.6 V Figure 10	-1		1	µA
On-Leakage Current	I <sub>ON</sub>	VCC = 4.3V, RST, DAT, CLK, VSIM = 0.3 V or 3.6 V	-1		1	µA
<b>SEL DIGITAL INPUTS</b>						
Input-Logic High	V <sub>IH</sub>	VCC = 1.65V to 5.0V,	1.7			V
Input-Logic Low	V <sub>IL</sub>	VCC = 1.65V to 5.0V,			0.4	V
Input Current Leakage	I <sub>IN</sub>	V <sub>IN</sub> = 0 or VCC	-1		1	µA

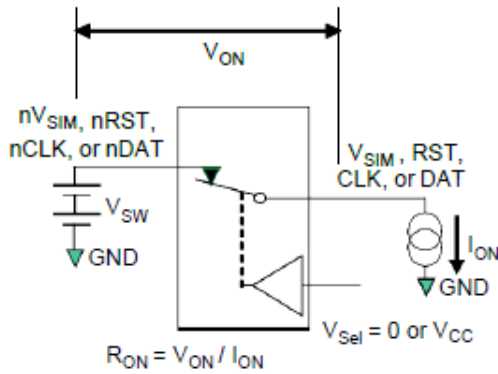
### Electrical Characteristics (continued)

(unless otherwise noted. Typical values are at  $V_{CC} = 3.3V$ ,  $T_A = +25^{\circ}C$ .) (2)

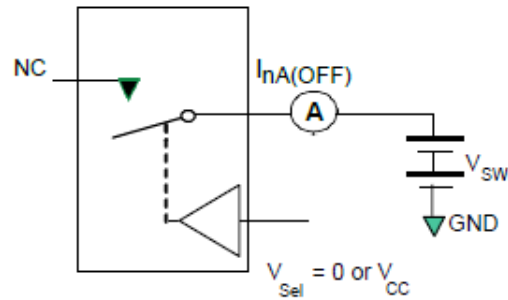
Parameter	Symbol	Conditions	Min	Typ	Max	Units	
<b>DYNAMIC CHARACTERISTICS</b>							
Turn-On Time Sel to Output (DAT,CLK,RST)	$T_{ON}$	$R_L = 50 \Omega$ , $C_L = 35$ Pf, $V_{SW} = 1.5 V$ , Figure 11, Figure 12	$T_A = +25^{\circ}C$		35	50	ns
			$T_A = T_{MIN}$ to $T_{MAX}$			60	
Turn-Off Time Sel to Output (DAT,CLK,RST)	$T_{OFF}$	$R_L = 50 \Omega$ , $C_L = 35$ pF, $V_{SW} = 1.5 V$ , Figure 11, Figure 12	$T_A = +25^{\circ}C$		15	40	ns
			$T_A = T_{MIN}$ to $T_{MAX}$			50	
Break-Before-Make Time (DAT,CLK,RST)	$t_{BBM}$	$R_L = 50 \Omega$ , $C_L =$ $35 pF$ $V_{SW1} =$ $V_{SW2} = 1.5 V$ Figure 15	$T_A = +25^{\circ}C$	2	15		ns
			$T_A = T_{MIN}$ to $T_{MAX}$	2			
Charge Injection	$Q$	$C_L = 50 pF$ , $R_{GEN} = 0 \Omega$ , $V_{GEN} = 0 V$		100		pC	
On-Channel Bandwidth -3dB (DAT,CLK,RST)	$BW$	$R_L = 50 \Omega$ , $C_L = 5 pF$ Figure 16		100		MHz	
Off-Isolation (DAT,CLK,RST)	$V_{ISO}$	$R_L = 50 \Omega$ , $f = 100KHz$ Figure 17		-66		dB	
Crosstalk	$V_{CT}$	$R_L = 50 \Omega$ , $f = 100KHz$ Figure 18		-86		dB	
RST, CLK, DAT Off Capacitance	$C_{OFF}$	$V_{CC} = 3.3 V$ , Figure 19		30		pF	
RST, CLK, DAT On Capacitance	$C_{ON}$	$V_{CC} = 3.3 V$ , $f = 1 MHz$ Figure 20		100		pF	

Note 2: Devices are 100% tested at  $T_A = +25^{\circ}C$ . Limits across the full temperature range are guaranteed by design and correlation.

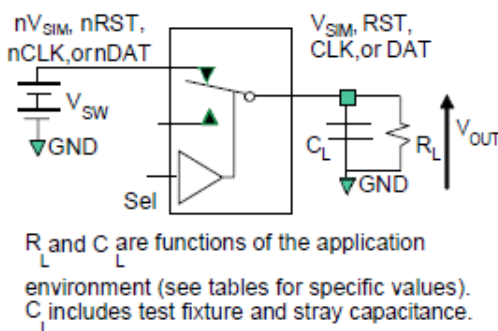
### Test Diagrams / Timing Diagrams



**Figure 9. On Resistance**

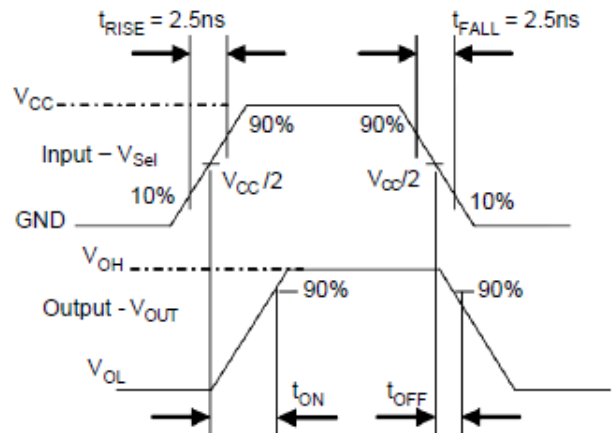


**Figure 10. Off Leakage**

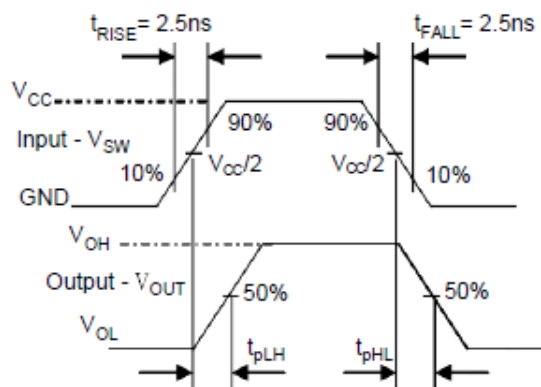


$R_L$  and  $C_L$  are functions of the application environment (see tables for specific values).  $C_L$  includes test fixture and stray capacitance.

**Figure 11. AC Test Circuit Load**



**Figure 12. Turn-On / Turn-Off Waveforms**



**Figure 13. Propagation Delay**

### Test Diagrams /Timing Diagrams

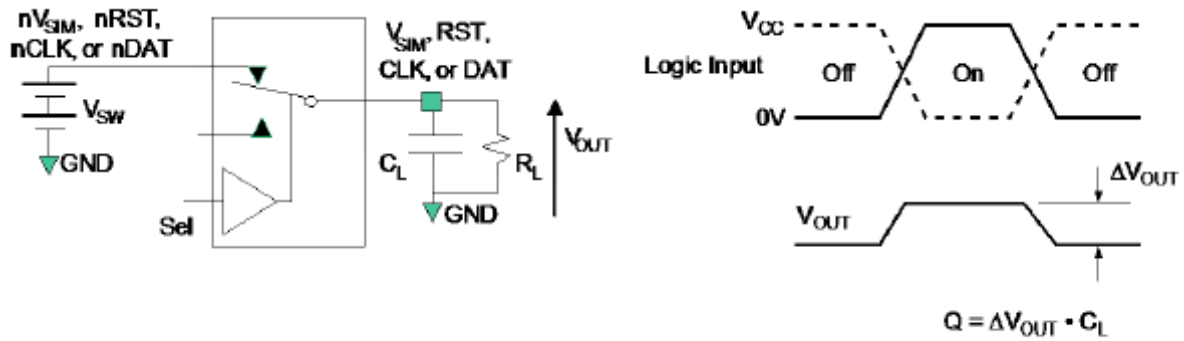
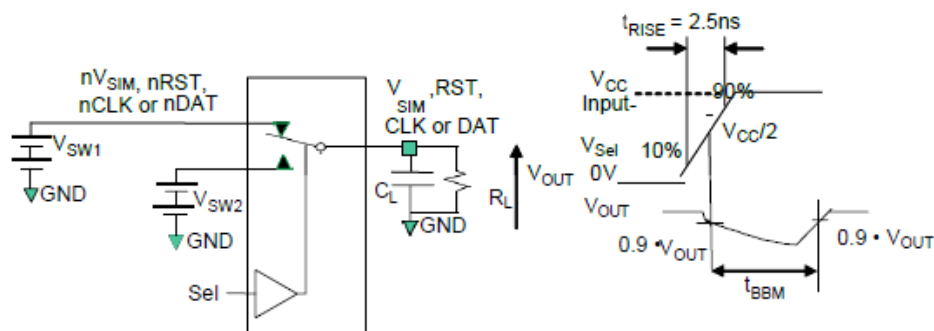
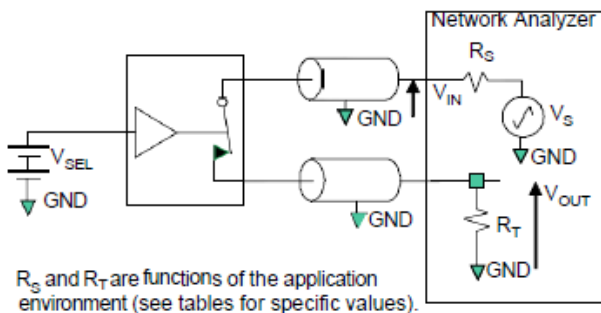


Figure 14. Charge Injection



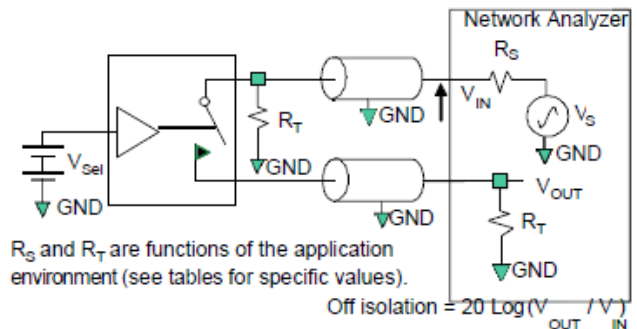
$R_L$  and  $C_L$  are functions of the application environment (see tables for specific values).  
 $C_L$  includes test fixture and stray capacitance.

Figure 15. Break-Before-Make Interval Timing



$R_S$  and  $R_T$  are functions of the application environment (see tables for specific values).

Figure 16. Bandwidth

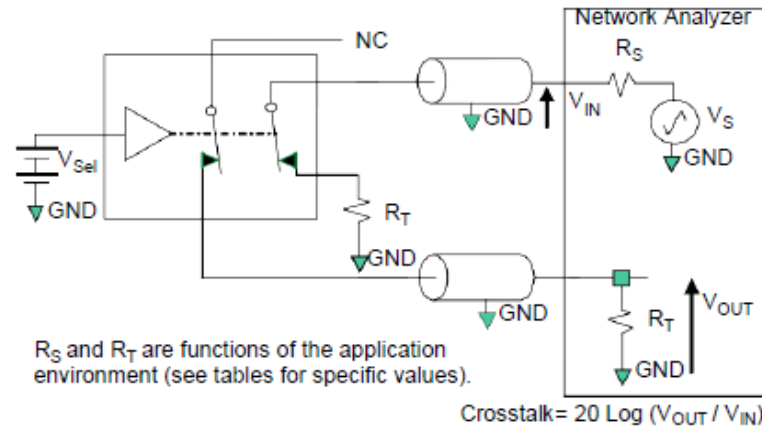


$R_S$  and  $R_T$  are functions of the application environment (see tables for specific values).

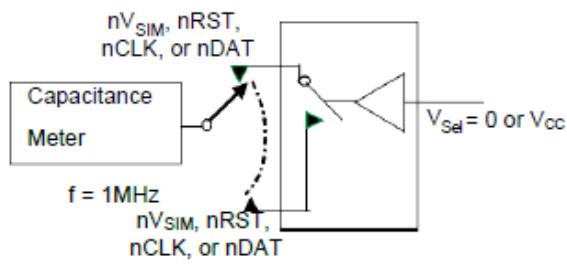
$$\text{Off isolation} = 20 \log(V_{\text{OUT}} / V_{\text{IN}})$$

Figure 17. Channel Off Isolation

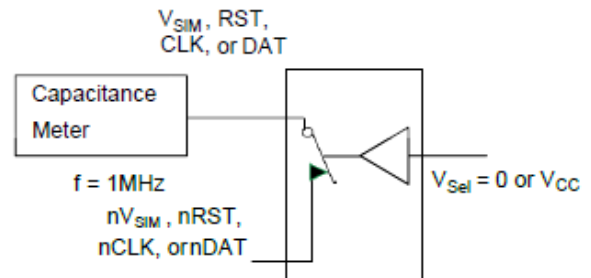
### Test Diagrams /Timing Diagrams



**Figure 18. Non-Adjacent Channel-to-Channel Crosstalk**



**Figure 19. Channel Off Capacitance**

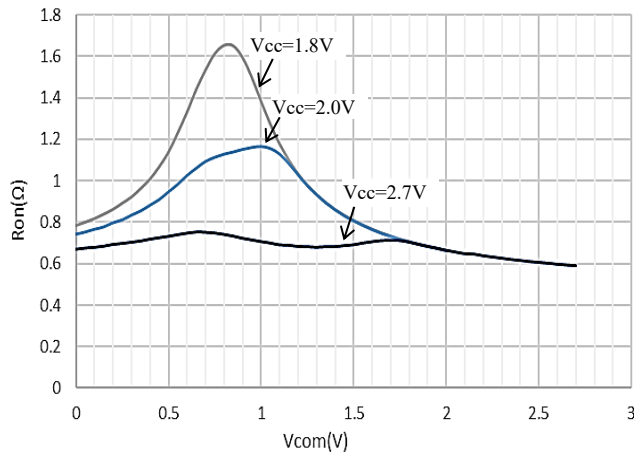


**Figure 20. Channel On Capacitance**

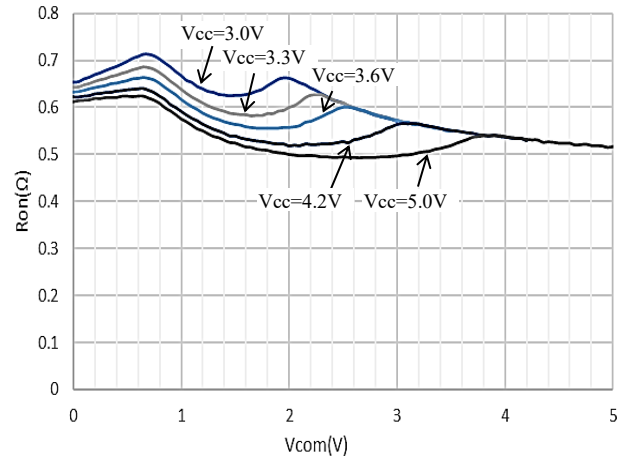
### Typical Operating Characteristics

(VCC = 3V, TA = +25°C, unless otherwise noted.)

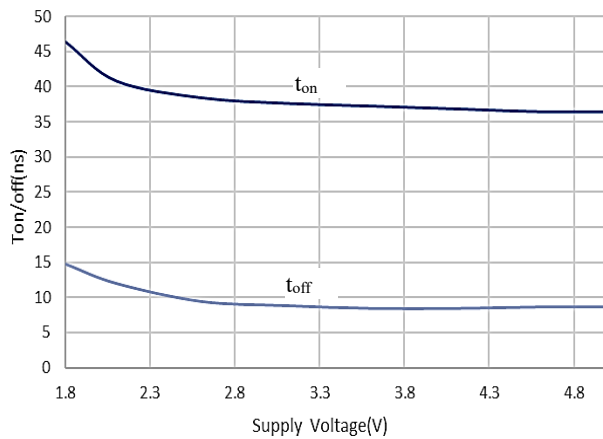
ON-RESISTANCE vs. COM\_ VOLTAGE



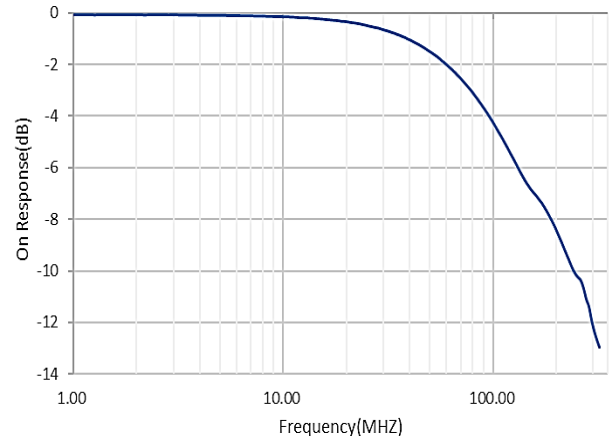
ON-RESISTANCE vs. COM\_ VOLTAGE



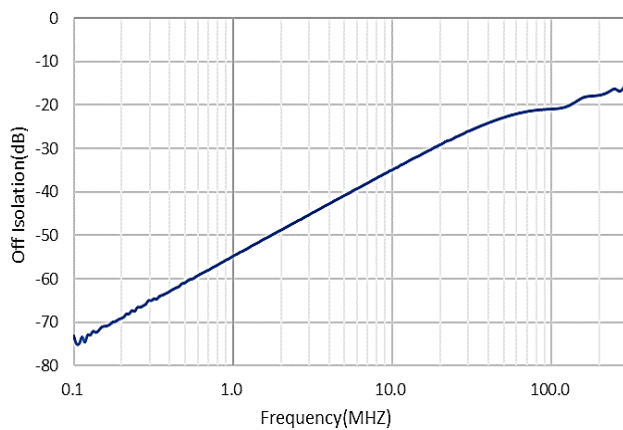
TURN-ON/OFF TIME vs. SUPPLY VOLTAGE



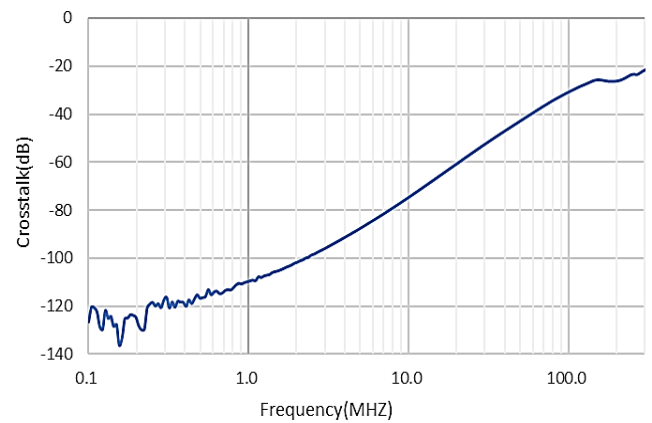
ON-RESPONSE vs. FREQUENCY



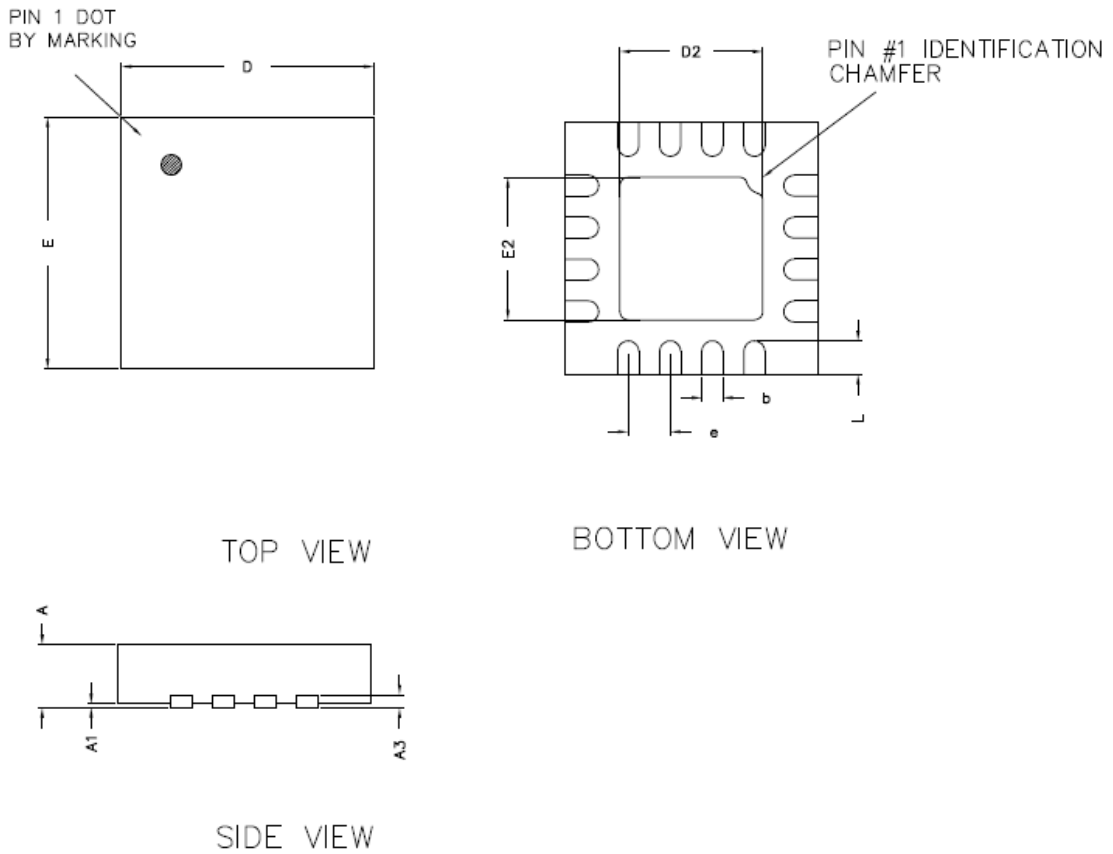
OFF-ISOLATION vs. FREQUENCY



CROSSTALK vs. FREQUENCY

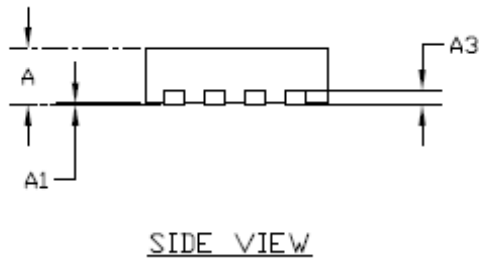
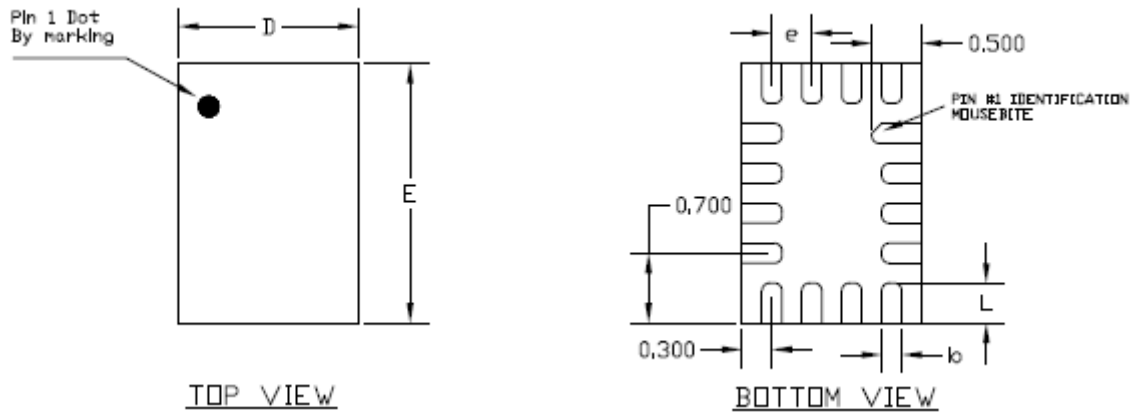


### PACKAGE OUTLINE DIMENSIONS: TQFN 3x3 -16L



COMMON DIMENSIONS(MM)			
PKG.	W: VERY VERY THIN		
REF.	MIN.	NOM.	MAX
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3	0.2 REF.		
D	2.95	3.00	3.05
E	2.95	3.00	3.05
b	0.18	0.25	0.30
L	0.30	0.40	0.50
D2	1.55	1.70	1.80
E2	1.55	1.70	1.80
e	0.5 BSC		

### PACKAGE OUTLINE DIMENSIONS: QFN2.6x1.8-16L



COMMON DIMENSIONS(MM)			
PKG.	UT:ULTRA THIN		
REF.	MIN.	NOM.	MAX
A	>0.50	0.55	0.60
A1	0.00	-	0.05
A3	0.15 REF.		
D	1.75	1.80	1.85
E	2.55	2.60	2.65
L	0.30	0.40	0.50
b	0.15	0.20	0.25
e	0.40 BSC		