

BCT647

2:1 MIPI C-PHY, D-PHY(4.5Gbps) 4-Data Lane Switch

GENERAL DESCRIPTION

The BCT647 is a four-data-lane MIPI D-PHY, C-PHY switch. This single-pole, double-throw (SPDT) switch is optimized for switching between two high-speed or low-power MIPI sources. The BCT647 is designed for the MIPI specification and allows connection to a CSI or DSI module.

APPLICATIONS

Cellular Phones, Smart Phones

Displays


Tablets

Laptops

FEATURES

- Switch Type: SPDT(10x)
- Signal Types: MIPI D-PHY, C-PHY
- V_{CC} : 1.5 to 5.0V
- Input Signals: 0 to 1.3V
- R_{ON} : 6.5 Ω Typical HS MIPI
6.5 Ω Typical LP MIPI
- ΔR_{ON} : 0.15 Ω Typical HS & LP MIPI
- R_{ON_FLAT} : 0.2 Ω Typical
- I_{CCZ} : 1uA Maximum
- I_{CC} : 35uA Maximum
- O_{IRR} : -25dB Typical
- X_{TALK} : -30dB Typical
- Differential Bandwidth: 4.5 GHz Typical
- Channel-to-Channel Skew: 6ps Typical
- C_{ON} : 1.5pF
- QFN4x4-38L Package

ORDERING INFORMATION

Order Number	Package Type	Temperature Range	Marking	QTY/Reel
BCT647EGU-TR	QFN4x4-38L	-40°C to +85°C	 WKL XXXXXX	5000

Mark Note: "XXXXXX" in Marking will be appeared as the batch code.

TYPICAL OPERATING CIRCUIT

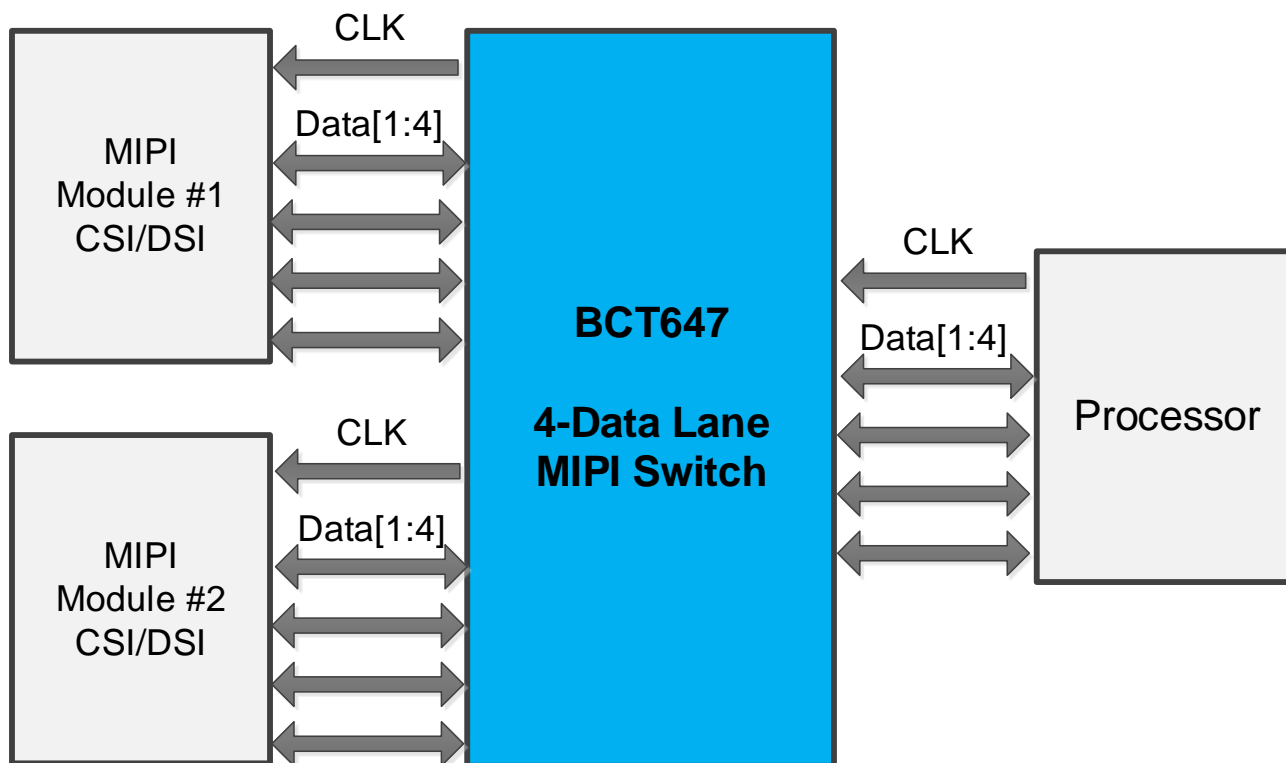


Figure 1. Application Block Diagram

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V _{CC})	-0.5V to +5.25V
DC Input Voltage (SEL, /OE) ⁽¹⁾	-0.5V to V _{CC} V
DC Switch I/O Voltage	-0.5V to 5.25V
DC Input Diode Current	-50mA
DC Output Current	50mA
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
Operating Temperature Range	-40°C to +85°C
Lead Temperature (Soldering, 10 sec)	260°C
ESD Susceptibility	
HBM All Pins	4KV

CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. Broadchip recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Broadchip reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact Broadchip sales office to get the latest datasheet.

RECOMMENDED OPERATING CONDITONS

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications.

Symbol	Parameter		Min.	Max.	Unit
V _{CC}	Supply Voltage		1.5	5.0	V
V _{CTRL}	Control Input Voltage(SEL, /OE) ⁽²⁾		0	V _{CC}	V
V _{SW}	Switch I/O Voltage (CLKn, CLKA _n , CLKB _n , D _n , DAn, DBn)	HS Mode	0	0.3	V
		LP Mode	0	1.3	
T _A	Operating Temperature		-40	+85	°C

Notes:

1. The input and output negative ratings maybe exceed if the input and output diode current ratings are observed.
2. The control input must be held HIGH or LOW; it must not float.

TRUTH TABLE

SEL	/OE	Function
LOW	LOW	CLKP=CLKAP, CLKN=CLKAN, D _N (P/N)=D _{AN} (P/N)
HIGH	LOW	CLKP=CLKBP, CLKN=CLKBN, D _N (P/N)=D _{BN} (P/N)
X	HIGH	Clock and Data Ports High Impedance

PIN CONFIGURATION (Top View)

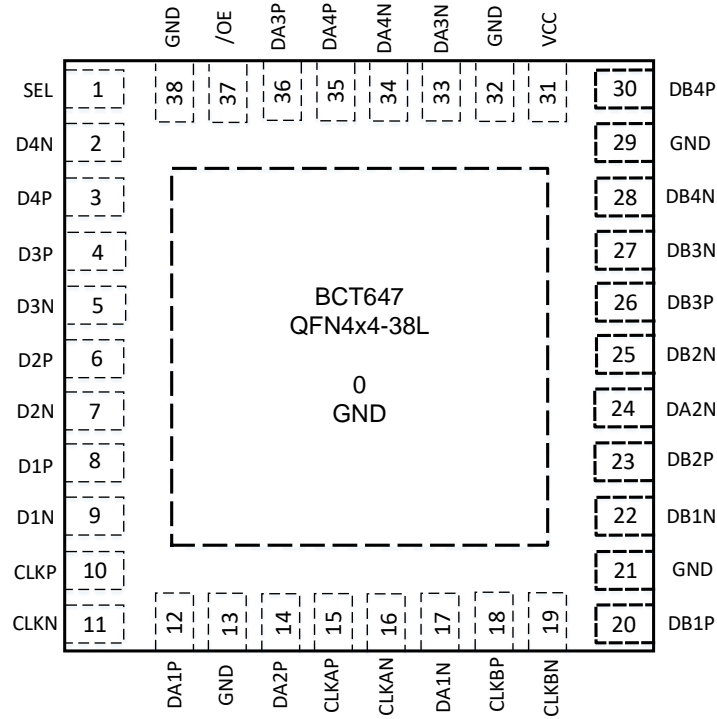


Figure2. Pin Configuration (Top Through View)

PIN	Pin Name	PIN	Pin Name	PIN	Pin Name
0,13,21,29,32,38	GND	14	DA2P	28	DB4N
1	SEL	15	CLKAP	30	DB4P
2	D4N	16	CLKAN	31	VCC
3	D4P	17	DA1N	33	DA3N
4	D3P	18	CLKBP	34	DA4N
5	D3N	19	CLKBN	35	DA4P
6	D2P	20	DB1P	36	DA3P
7	D2N	22	DB1N	37	/OE
8	D1P	23	DB2P		
9	D1N	24	DA2N		
10	CLKP	25	DB2N		
11	CLKN	26	DB3P		
12	DA1P	27	DB3N		

Table 1. Pin Mappings

PIN DESCRIPTION

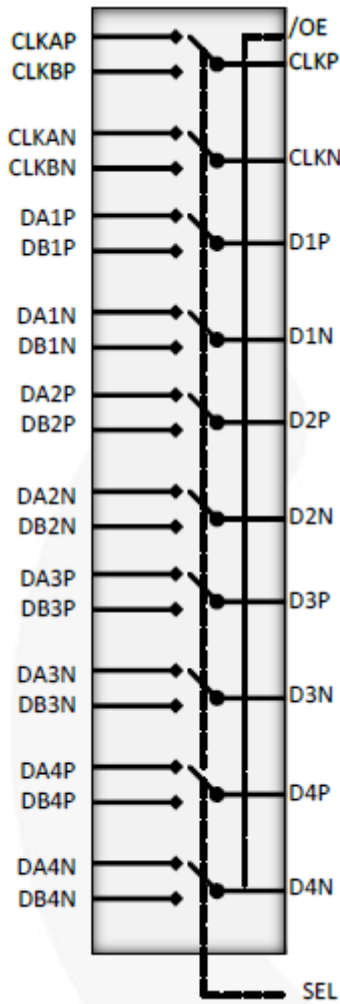


Figure 3. Analog Symbol

Pin Name	Description	
CLKP/N	Common Clock Path	
D1P/N	Common Data Path1	
D2P/N	Common Data Path2	
D3P/N	Common Data Path3	
D4P/N	Common Data Path4	
CLKAP/N	A-Side Clock Path	
DA1P/N	A-Side Data Path 1	
DA2P/N	A-Side Data Path 2	
DA3P/N	A-Side Data Path 3	
DA4P/N	A-Side Data Path 4	
CLKBP/N	B-Side Clock Path	
DB1P/N	B-Side Data Path 1	
DB2P/N	B-Side Data Path 2	
DB3P/N	B-Side Data Path 3	
DB4P/N	B-Side Data Path 4	
SEL	SEL=0	CLKP=CLKAP, CLKN=CLKAN, Dn(P/N)=DAn(P/N)
	SEL=1	CLKP=CLKBP, CLKN=CLKBN, Dn(P/N)=DBn(P/N)
/OE	Output Enable	
VCC	Power	
GND	Ground	

DC ELECTRICAL CHARACTERISTICS

(All typical values are $T_A = 25^{\circ}\text{C}$, unless otherwise specified.)

PARAMETER	SYM	CONDITIONS	V_{CC} (V)	MIN	TYP	MAX	UNITS
Control Input Leakage(SEL, /OE)	I_{IN}	$V_{CNTRL}=0$ to V_{CC}	5.0	-1		1	μA
Input Voltage High	V_{IH}	SEL, /OE	1.5 to 5.0	1.4			V
Input Voltage Low	V_{IL}	SEL, /OE	1.5 to 5.0			0.4	V
Off leakage Current of Port CLKAn, DAn, CLKBn, DBn	$I_{NO(OFF)}$ $I_{NC(OFF)}$	$V_{SW}=0 \leq \text{DATA} \leq 1.3\text{V}$	5.0	-1		1	μA
On leakage Current of Common Ports(CLK _n , D _n)	$I_{A(ON)}$	$V_{SW}=0 \leq \text{DATA} \leq 1.3\text{V}$	5.0	-1		1	μA
Power-Off Leakage Current (All I/O Ports)	I_{OFF}	$V_{SW}=0$ or 1.3V	0	-1		1	μA
Off-State Leakage	I_{OZ}	$V_{SW}=0 \leq \text{DATA} \leq 1.3\text{V}$, /OE=High	5.0	-1		1	μA
Switch On Resistance for HS MIPI Applications ⁽³⁾	$R_{ON_MIPI_HS}$	$I_{ON}=-8\text{mA}$, /OE=0V, SEL= V_{CC} or 0V, CLKA, CLKB, DBn or DAn=0.3V	1.5 to 5.0		6.5	9	Ω
Switch On Resistance for LP MIPI Applications ⁽³⁾	$R_{ON_MIPI_LP}$	$I_{ON}=-8\text{mA}$, /OE=0V, SEL= V_{CC} or 0V, CLKA, CLKB, DBn or DAn=1.3V	1.5 to 5.0		6.5	9	Ω
On Resistance Matching Between HS MIPI Channels ⁽⁴⁾	$\Delta R_{ON_MIPI_HS}$	$I_{ON}=-8\text{mA}$, /OE=0V, SEL= V_{CC} or 0V, CLKA, CLKB, DBn or DAn=0.3V	1.5 to 5.0		0.15		Ω

DC ELECTRICAL CHARACTERISTICS

(All typical values are $T_A = 25^\circ\text{C}$, unless otherwise specified.)

PARAMETER	SYM	CONDITIONS	V_{CC} (V)	MIN	TYP	MAX	UNITS
On Resistance Matching Between LP MIPI Channels ⁽⁴⁾	$\Delta R_{ON_MIPI_LP}$	$I_{ON}=-8\text{mA}$, $/OE=0\text{V}$, $SEL=V_{CC}$ or 0V , $CLKA$, $CLKB$, DBn or $DAn=1.3\text{V}$	1.5 to 5.0		0.15		Ω
On Resistance Flatness for HS MIPI Signals ⁽⁴⁾	$R_{ON_FLAT_MIPI_HS}$	$I_{ON}=-8\text{mA}$, $/OE=0\text{V}$, $SEL=V_{CC}$ or 0V , $CLKA$, $CLKB$, DBn or $DAn=0$ to 0.3V	1.5 to 5.0		0.2		Ω
On Resistance Flatness for LP MIPI Signals ⁽⁴⁾	$R_{ON_FLAT_MIPI_LP}$	$I_{ON}=-8\text{mA}$, $/OE=0\text{V}$, $SEL=V_{CC}$ or 0V , $CLKA$, $CLKB$, DBn or $DAn=0$ to 1.3V	1.5 to 5.0		0.2		Ω
Quiescent Hi-Z Supply Current	I_{CCZ}	$V_{SEL}=0$ or V_{CC} , $I_{OUT}=0$, $/OE=V_{CC}$	5.0			1	μA
Quiescent Supply Current (Includes Charge Pump)	I_{CC}	$V_{SEL}=0$ or V_{CC} , $I_{OUT}=0$, $/OE=0\text{V}$	5.0			35	μA

Notes:

3. Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the two (A or B ports).

4. Guaranteed by characterization

AC ELECTRICAL CHARACTERISTICS

(All values are for $V_{CC}=3.3\text{V}$ at $T_A=25^\circ\text{C}$, unless otherwise specified.)

PARAMETER	SYM	CONDITIONS	V_{CC} (V)	MIN	TYP	MAX	UNITS
Initialization Time VCC to Output ⁽⁵⁾	t_{INIT}	$R_L=50\Omega$, $C_L=0\text{pF}$, $V_{SW}=0.6\text{V}$	1.5 to 5.0		60		μs
Enable Turn-On Time, $/OE$ to Output	t_{EN}	$R_L=50\Omega$, $C_L=0\text{pF}$, $V_{SW}=0.6\text{V}$	1.5 to 5.0		60	150	μs
Disable Turn-off Time, $/OE$ to Output	t_{DIS}	$R_L=50\Omega$, $C_L=0\text{pF}$, $V_{SW}=0.6\text{V}$	1.5 to 5.0		35	250	ns
Turn-On Time SEL to Output	t_{ON}	$R_L=50\Omega$, $C_L=0\text{pF}$, $V_{SW}=0.6\text{V}$	1.5 to 5.0		350	1350	ns

AC ELECTRICAL CHARACTERISTICS

(All values are for $V_{CC}=3.3V$ at $T_A=25^{\circ}C$, unless otherwise specified.)

PARAMETER	SYM	CONDITIONS	V_{CC} (V)	MIN	TYP	MAX	UNITS
Turn-Off Time SEL to Output	t_{OFF}	$R_L=50\Omega$, $C_L=0pF$, $V_{SW}=0.6V$	1.5 to 5.0		125	1150	ns
Break-Before-Make Time	t_{BBM}	$R_L=50\Omega$, $C_L=0pF$, $V_{SW}=0.6V$	1.5 to 5.0	50		450	ns
Propagation Delay(5)	t_{PD}	$C_L=0pF$, $R_L=50\Omega$	1.5 to 5.0		0.25		ns
Off Isolation for MIPI(5)	O_{IRR}	$f=1250MHz$, $R_L=50\Omega$, /OE=HIGH, $V_{SW}=200mV_{PP}$	1.5 to 5.0		-25		dB
Crosstalk for MIPI(5)	X_{TALK}	$f=1250MHz$, $R_L=50\Omega$, /OE=Low, $V_{SW}=200mV_{PP}$	1.5 to 5.0		-30		dB
Differential -3dB Bandwidth(5)	BW	$C_L=0pF$, $R_L=50\Omega$, $V_{SW}=200mV_{PP}$	1.5 to 5.0	3.5	4.5		GHz

Note:

5. Guaranteed by characterization.

HIGH-SPEED-RELATED AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYM	CONDITIONS	V_{CC} (V)	MIN	TYP	MAX	UNITS
HS Mode Skew of Opposite Transitions of the Same Output ⁽⁶⁾	$t_{SK(P)}$	$R_L=50\Omega$, $C_L=0pF$, $V_{SW}=0.3V$	1.5 to 5.0		6		ps

Note:

6. Guaranteed by characterization.

CAPACITANCE

PARAMETER	SYM	CONDITIONS	V_{CC} (V)	MIN	TYP	MAX	UNITS
Control Pin Input Capacitance ⁽⁷⁾	C_{IN}	$V_{CC}=0V$, $f=1MHz$	0		2.1		pF
Output On Capacitance ⁽⁷⁾	C_{ON}	$V_{CC}=3.3V$, /OE=0V, $f=1250MHz$ (In HS common value)	3.3		1.5		
Output Off Capacitance ⁽⁷⁾	C_{OFF}	V_{CC} and /OE=3.3V, $f=1250MHz$ (Both sides in HS common value)	3.3		0.9		

Note:

7. Guaranteed by characterization.

TEST DIAGRAMS

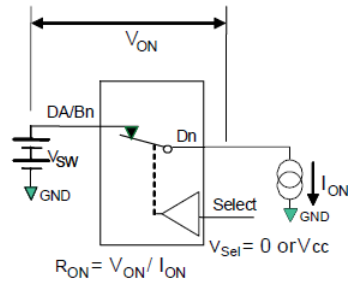
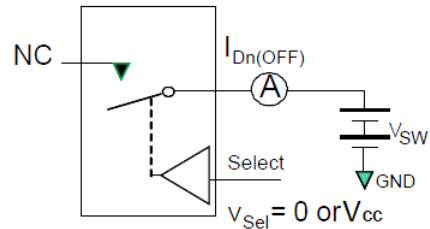


Figure 4. On Resistance



**Each switch port is tested separately

Figure 5. Off Leakage

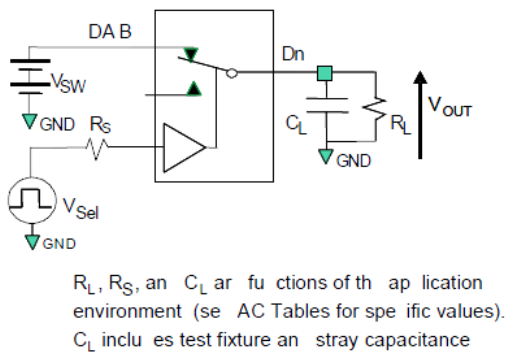


Figure 6. AC Test Circuit Board

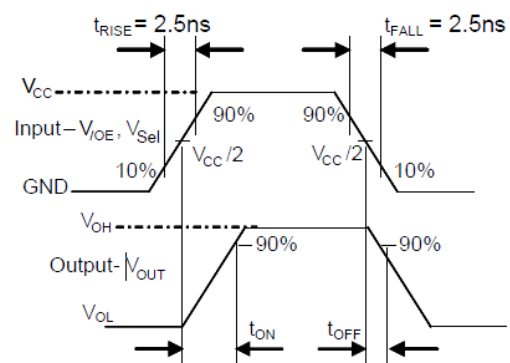


Figure 7. Turn-On/Turn-Off waveform

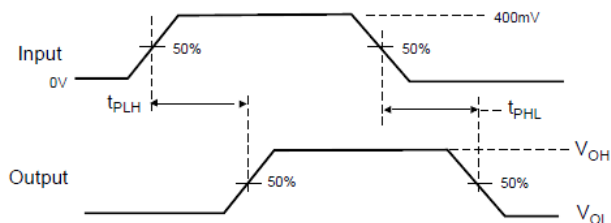


Figure 8. Propagation Delay(t_{PLH} -500ps)

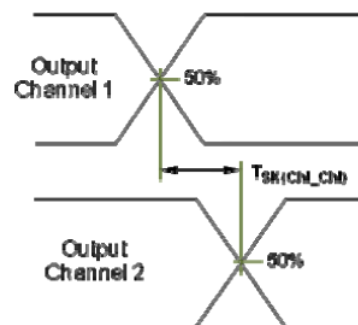


Figure 9. Channel to Channel Skew

TEST DIAGRAMS(CONTINUED)

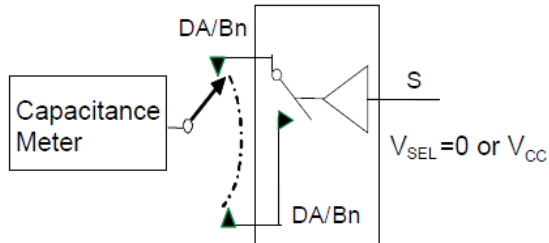


Figure 10. Channel Off Capacitance

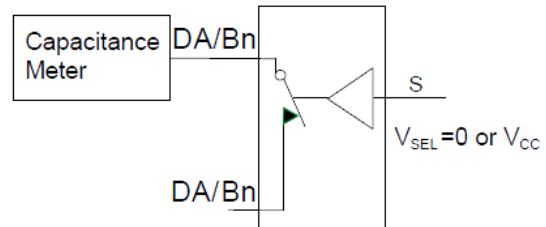


Figure 11. Channel On Capacitance

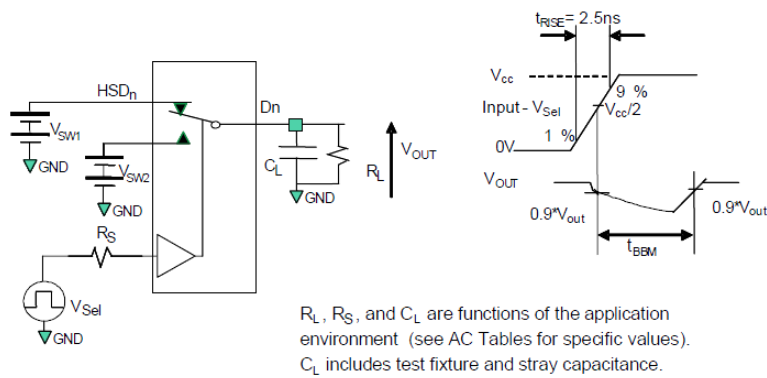
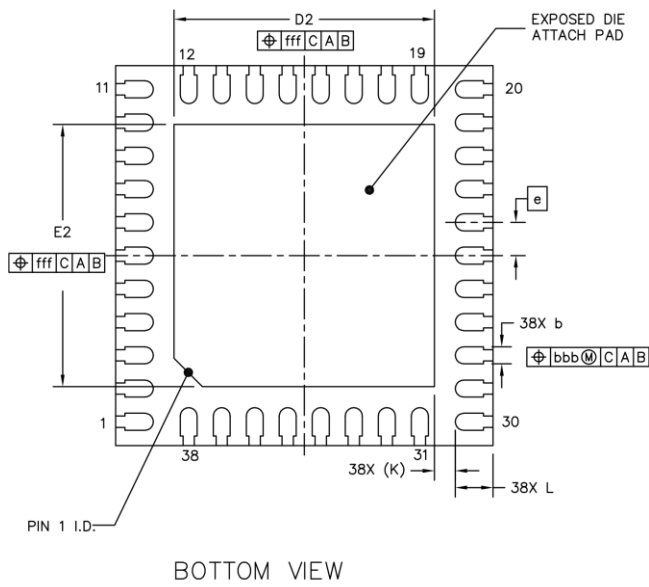
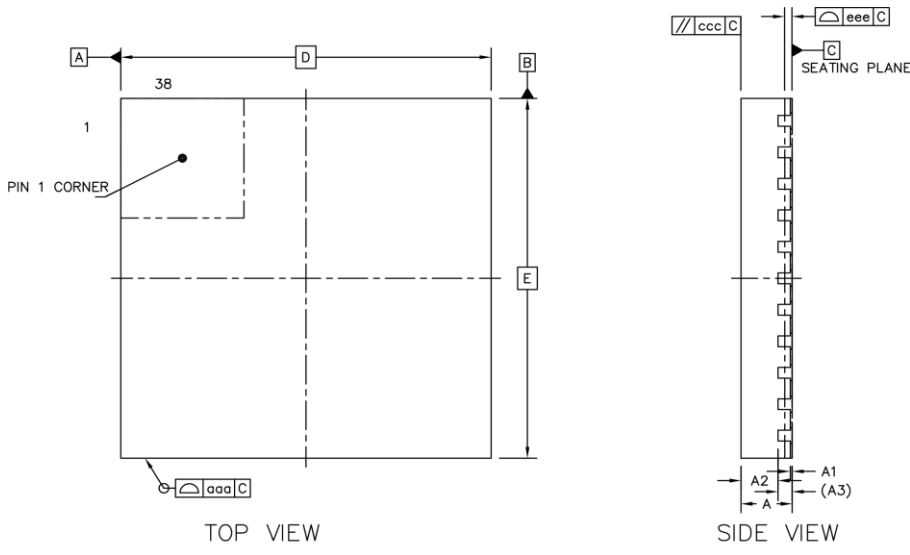


Figure 12. Break-Before-Make Interval Timing

PACKAGE OUTLINE DIMENSIONS



	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.5	0.55	0.6
STAND OFF	A1	0	0.02	0.05
MOLD THICKNESS	A2	---	0.4	---
L/F THICKNESS	A3	0.152 REF		
LEAD WIDTH	b	0.13	0.18	0.23
BODY SIZE	X	D		
	Y	E		
LEAD PITCH	e	0.35 BSC		
EP SIZE	X	D2	2.66	2.76
	Y	E2	2.66	2.76
LEAD LENGTH	L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE	K	0.22 REF		
PACKAGE EDGE TOLERANCE	aaa	0.1		
MOLD FLATNESS	ccc	0.1		
COPLANARITY	eee	0.08		
LEAD OFFSET	bbb	0.07		
EXPOSED PAD OFFSET	fff	0.1		